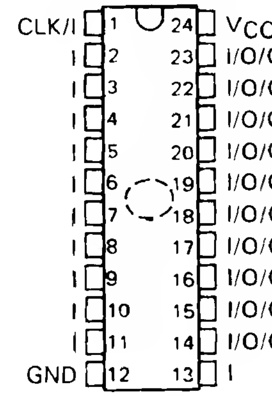
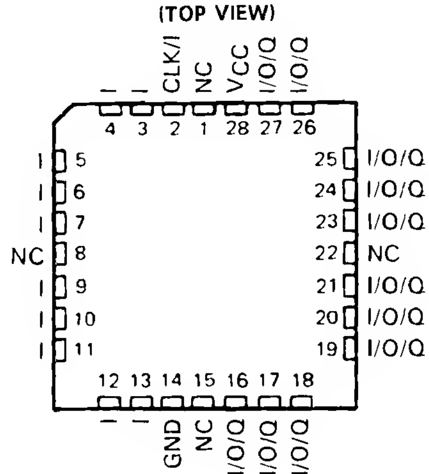
D3323, SEPTEMBER 1989—REVISED APRIL 1991

- 24-Pin Advanced CMOS PLD
- Virtually Zero Standby Power
- Propagation Delay Time
  - 25 ns . . . Turbo Mode
  - 35 ns . . . Zero-Power Mode
  - 15 ns . . . CLK-to-Q
- Variable Product Term Distribution Allows More Complex Functions to Be Implemented
- Each Output Is User-Programmable for Registered or Combinatorial Operation, Polarity, and Output Enable Control
- Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability
- Preload Capability on All Registered Outputs Allows for Improved Device Testing
- UV Light Erasable Cell Technology Allows for:
  - Reconfigurable Logic
  - Reprogrammable Cells
  - Full Factory Testing for Guaranteed 100% Yields
- Programmable Design Security Bit Prevents Copying of Logic Stored in Device
- Package Options Include Plastic DIP and Chip Carrier [for One-Time-Programmable (OTP) Devices] and Ceramic Dual-In-Line Windowed Package

JTL AND NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC—No internal connection
Pin assignments in operating mode

description

This CMOS PLD device features variable product terms, flexible outputs, and virtually zero standby power. It combines TI's EPIC ™ (Enhanced Processed Implanted CMOS) process with ultraviolet-light-erasable EPROM technology. Each output has an OLM (Output Logic Macrocell) configuration allowing for user definition of the output type. This device provides reliable, low-power substitutes for numerous high-performance TTL PLDs with gate complexities between 300 and 800 gates.

The 'PAL22V10Z has 12 dedicated inputs and ten user-definable outputs. Individual outputs can be programmed as registered or combinational and inverting or noninverting as shown in the Output Logic Macrocell (OLM) diagram. These ten outputs are enabled through the use of individual product terms.

The variable product-term distribution on this device removes rigid limitation to a maximum of eight product terms per output. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. The variable allocation of product terms allows for far more complex functions to be implemented in this device than in previously available devices.

This device is covered by U.S. Patent 4,410,987.
EPIC is a trademark of Texas Instruments Incorporated.

description (continued)

With features such as the programmable OLMs and the variable product-term distribution, the TICPAL22V10Z offers quick design and development of custom LSI functions. Since each of the ten output pins may be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs can be implemented with this device.

Design complexity is enhanced by the addition of synchronous set and asynchronous reset product terms. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0 independently of the clock. The output logic level after set or reset will depend on the polarity selected during programming.

Output registers of this device can be preloaded to any desired state during testing, thus allowing for full logical verification during product testing.

The TICPAL22V10Z has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015.6. However, care should be exercised in handling these devices, as exposure to ESD may result in a degradation of the device parametric performance.

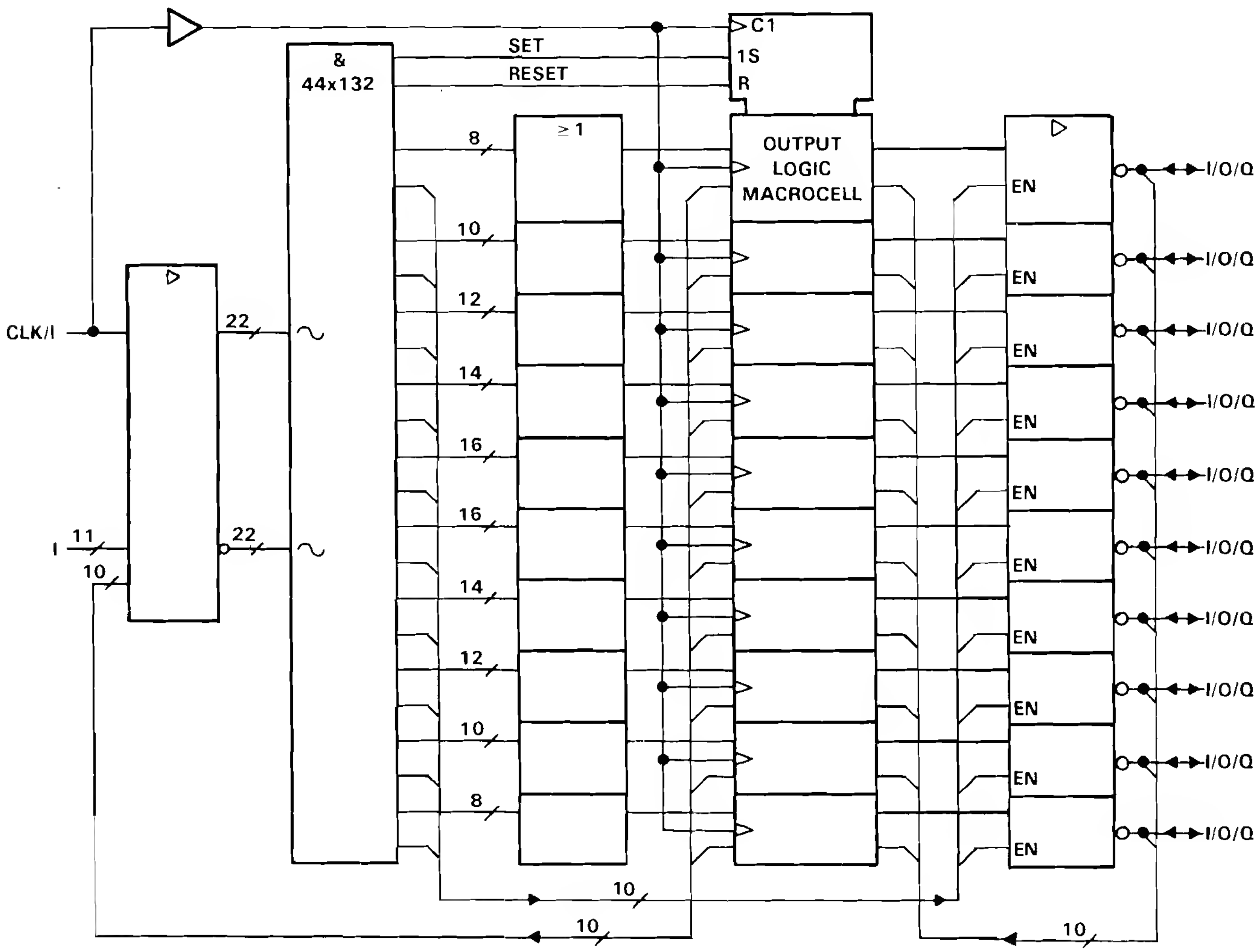
The floating gate programmable cells allow these PAL devices to be fully programmed and tested before assembly to assure high field programming yield and functionality. They are then erased by ultraviolet light before packaging.

The TICPAL22V10Z-25C and TICPAL22V10Z-35C are characterized for operation from 0 °C to 75 °C.

design security

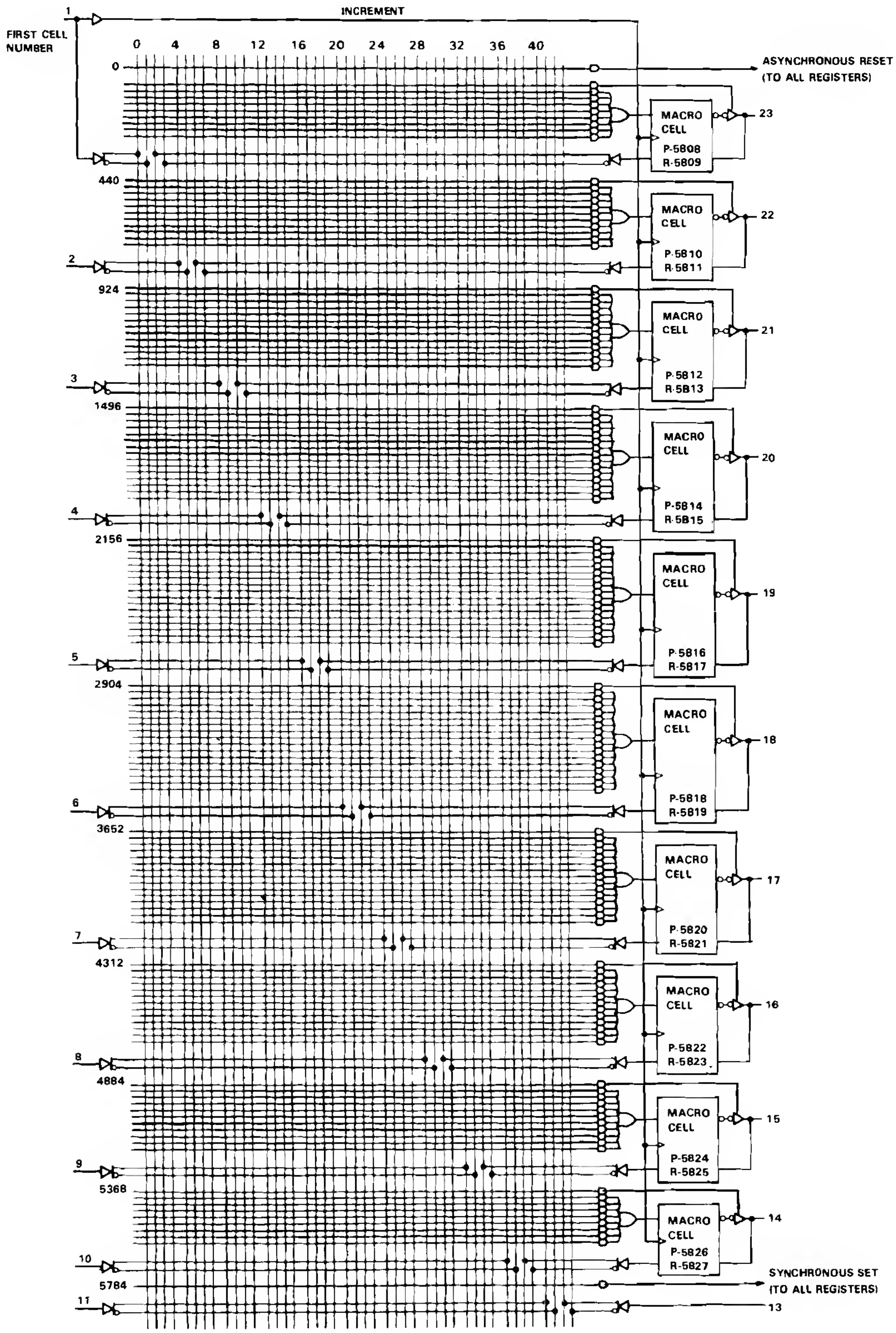
The 'PAL22V10Z contains a programmable design security cell. Programming this cell will disable the read verify and programming circuitry protecting the design from being copied. The security cell is usually programmed after the design is finalized and released to production. A secured device will verify as if every location in the device is programmed. Because programming is accomplished by storing an invisible charge instead of opening a metal link, the '22V10Z cannot be copied by visual inspection. Once a secured device is fully erased, it can be reprogrammed to any desired configuration.

functional block diagram (positive logic)



∿ denotes programmable cell inputs

logic diagram (positive logic)



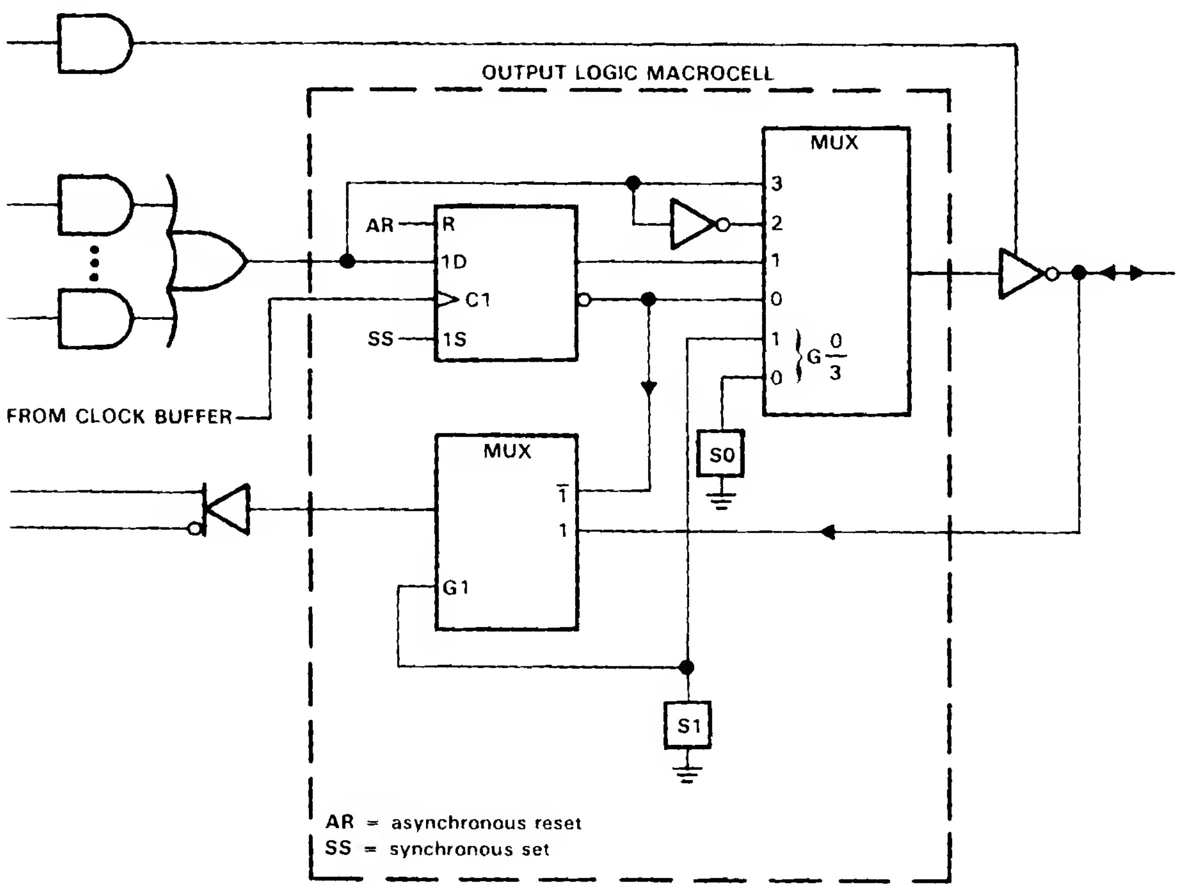
Programmable Cell Number = First Cell Number + Increment

output logic macrocell (OLM) description

A great amount of architectural flexibility is provided by the user-configurable macrocell output options. The macrocell consists of a D-type flip-flop and two select multiplexers. The D-type flip-flop operates like a standard TTL D-type flip-flop. The input data is latched on the low-to-high transition of the clock input. The Q and $\overline{Q}$ outputs are made available to the output select multiplexer. The asynchronous reset and synchronous set controls are available in all flip-flops.

The select multiplexers are controlled by programmable cells. The combination of these programmable cells will determine which macrocell functions are implemented. It is this user control of the architectural structure that provides the generic flexibility of this device.

output logic macrocell diagram

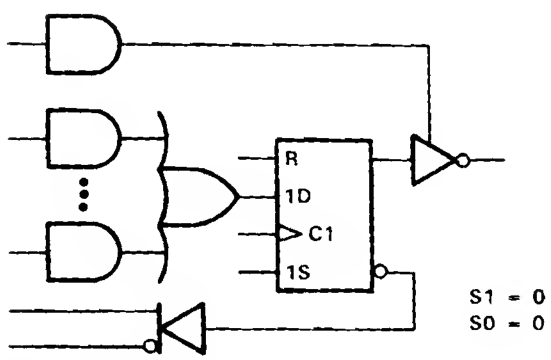


output logic macrocell options

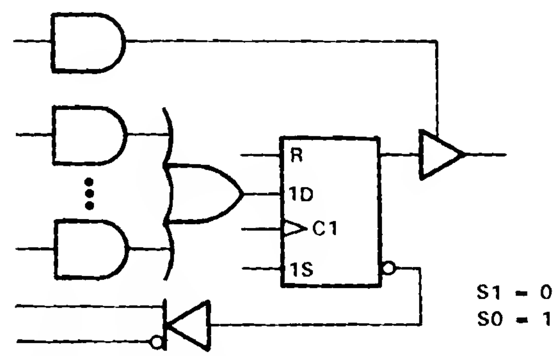
MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

CELL SELECT		FEEDBACK AND OUTPUT CONFIGURATION		
S1	S0			
0	0	Register feedback	Registered	Active low
0	1	Register feedback	Registered	Active high
1	0	I/O feedback	Combinational	Active low
1	1	I/O feedback	Combinational	Active high

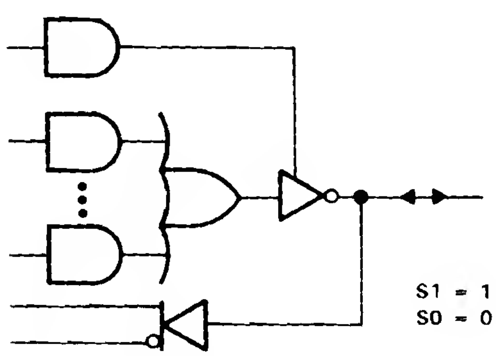
0 = erased cell   1 = programmed cell
S1 and S0 are select-function cells as shown in the output logic macrocell diagram.



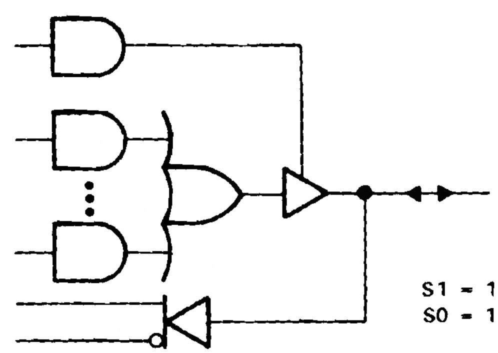
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

absoiute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 to V_{CC} + 0.5 V
Input diode current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) .... ±20 mA
Output diode current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) .... ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±40 mA
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: FN or NT package .... 260°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: JTL package .... 300°C
Operating free-air temperature range .... 0°C to 75°C
Storage temperature range .... −65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
Note 1: This rating applies except during programming and preload cycles.

recommended operating conditions

			−25C			−35C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	Driving TTL			−3.2			−3.2	mA
		Driving CMOS			−4			−4	
I_{OL}	Low-level output current	Driving TTL			16			16	mA
		Driving CMOS			4			4	
t_w	Pulse duration	CLK high	10			15			ns
		CLK low	10			15			ns
		Asynchronous reset	20			25			ns
t_{su}	Setup time, turbo mode	Input or feedback	17			25			ns
		Asynchronous reset inactive	20			30			
		Synchronous preset inactive	20			30			
t_{su}	Setup time, zero-power mode	Input or feedback	25			35			ns
		Asynchronous reset inactive	30			40			
		Synchronous preset inactive	30			40			
t_h	Hold time	Input or feedback	0			0			ns
T_A	Operating free-air temperature		0		75	0		75	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		-25C MIN	-25C TYP†	-25C MAX	-35C MIN	-35C TYP†	-35C MAX	UNIT
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = −3.2 mA for TTL	4	4.8		4	4.8		V
	V_{CC} = 4.75 V,	I_{OH} = −4 mA for CMOS	3.86	4.7		3.86	4.7		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 16 mA for TTL		0.25	0.5		0.25	0.5	V
	V_{CC} = 4.75 V,	I_{OL} = 4 mA for CMOS		0.07	0.4		0.07	0.4	V
I_{OZH}	V_{CC} = 5.25 V,	V_O = 2.7 V		0.01	10		0.01	10	μA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.5 V		−0.01	−10		−0.01	−10	μA
I_{IH}	V_{CC} = 5.25 V,	V_I = 5.25 V		0.01	10		0.01	10	μA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.5 V		−0.01	−10		−0.01	−10	μA
I_O‡	V_{CC} = 5.25 V,	V_O = 0.5 V	−30	−45	−90	−30	−45	−90	mA
I_{CC} (Zero-power mode)	V_{CC} = 5.25 V, Outputs open§	V_I = 0 or V_{CC},		10	100		10	100	μA
C_i	V_I = 2 V,	All inputs		6			6		pF
	f = 1 MHz	All I/O pins		10			10		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 4)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	-25C MIN	-25C TYP†	-25C MAX	-35C MIN	-35C TYP†	-35C MAX	UNIT
f_{max}¶	Without feedback			50	66		33	47		MHz
	With feedback			28.5	55		20	38		MHz
t_{pd}	Turbo mode	I, I/O	O, I/O		16	25		22	35	ns
	Zero-power mode	I, I/O	O, I/O		21	35		28	45	ns
t_{pd}	Turbo mode	Asynchronous RESET	Q		18	30		24	40	ns
	Zero-power mode	Asynchronous RESET	Q		23	40		31	50	ns
t_{pd}		CLK↑	Q		10	15		14	25	ns
t_{en}	Turbo mode	I, I/O	I, Q, I/O		15	25		21	35	ns
	Zero-power mode	I, I/O	I, Q, I/O		20	35		27	45	ns
t_{dis}	Turbo mode	I, I/O	I, Q, I/O		15	25		21	35	ns
	Zero-power mode	I, I/O	I, Q, I/O		17	35		25	45	ns

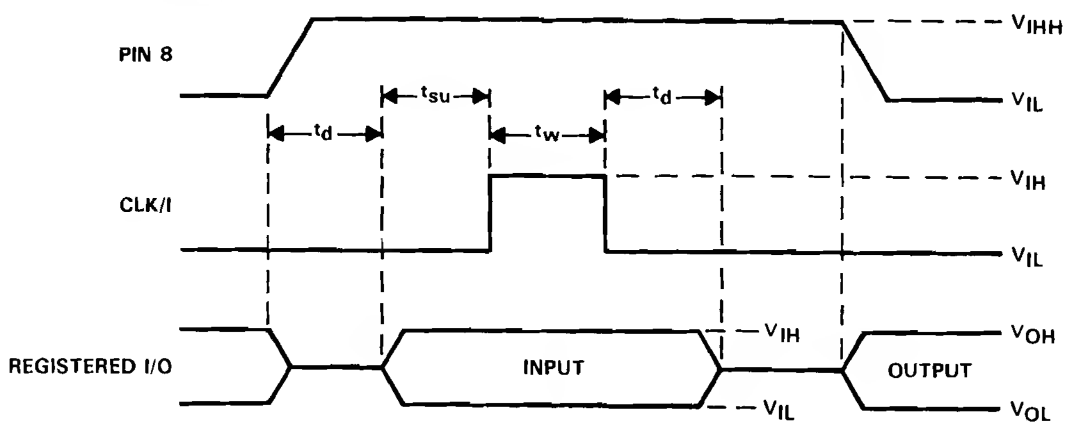
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡This parameter approximates I_{OS}. The condition V_O = 0.5 V takes tester noise into account.
§Disabled outputs are tied to GND or V_{CC}.
¶f_{max} (with feedback) $= \dfrac{1}{t_{su} + t_{pd}\text{ (CLK to Q)}}$; f_{max} (without feedback) $= \dfrac{1}{t_w\text{(hi)} + t_w\text{(low)}}$

preload procedure for registered outputs

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below. The output level depends on the polarity selected during programming.

Step 1. With V_{CC} at 5 volts and pin 1 at V_{IL}, raise pin 8 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 8 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

preload waveforms (see Note 2)



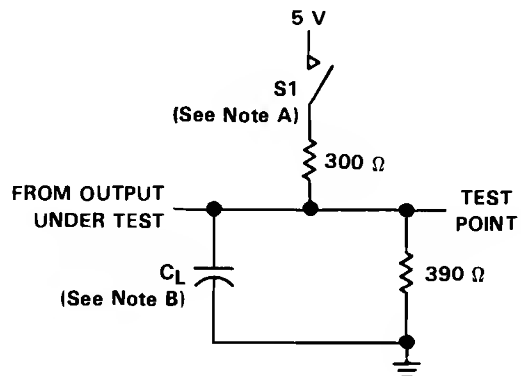
NOTE 2: $t_d = t_{su} = t_w =$ 100 ns to 1000 ns. $V_{IHH} =$ 10.25 V to 10.75 V.

programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

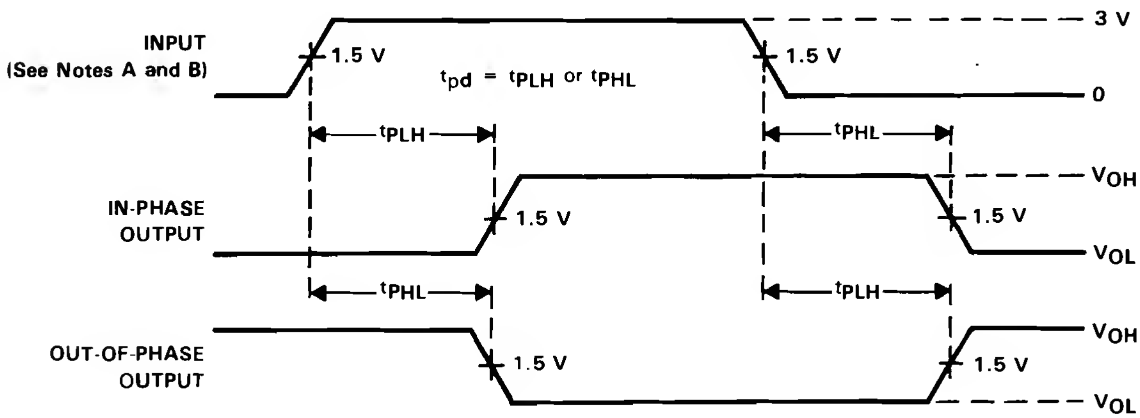
Complete programming specification, algorithms, and the lastest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. When measuring propagation times of 3-state outputs, S1 is closed.
B. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en} and 5 pF for t_{dis}.

FIGURE 1. LOAD CIRCUIT FOR THREE-STATE OUTPUTS

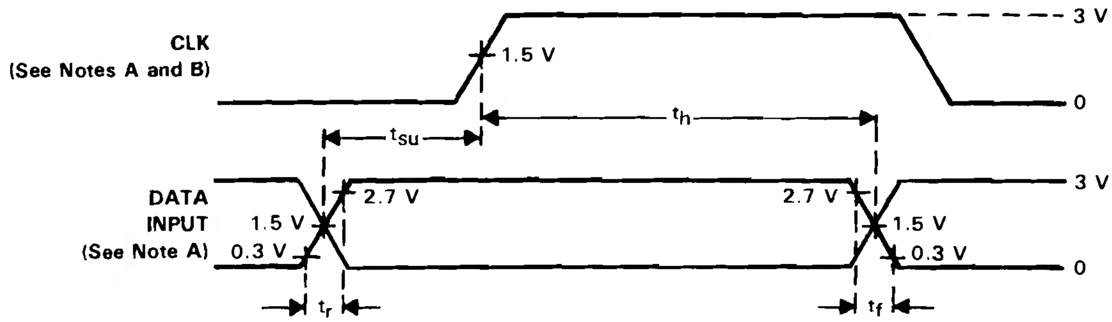


VOLTAGE WAVEFORMS

NOTES: A. When measuring propagation times of 3-state outputs, S1 is closed.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, $t_r = t_f$ = 2 ns.

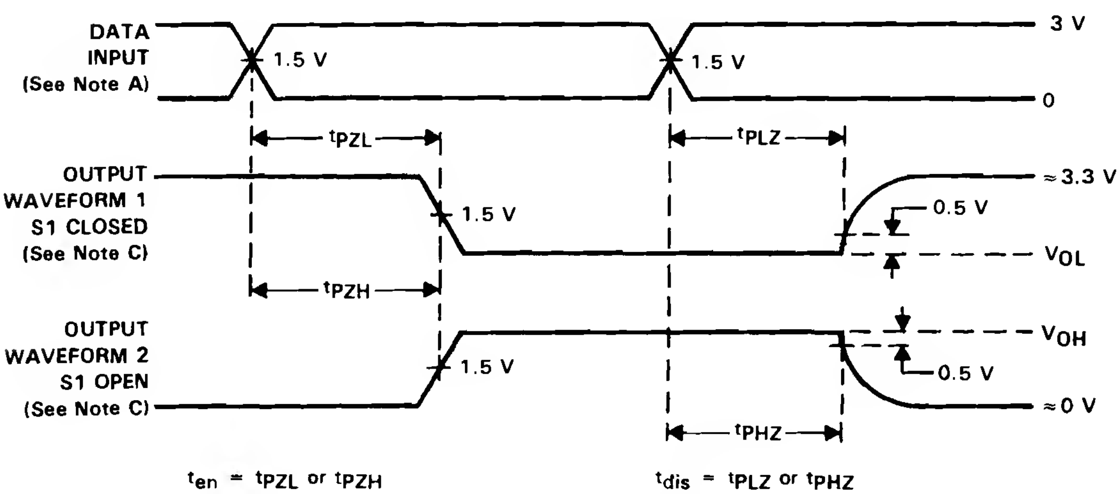
FIGURE 2. PROPAGATION DELAY TIMES, OUTPUT RISE AND FALL TIMES

PARAMETER MEASUREMENT INFORMATION



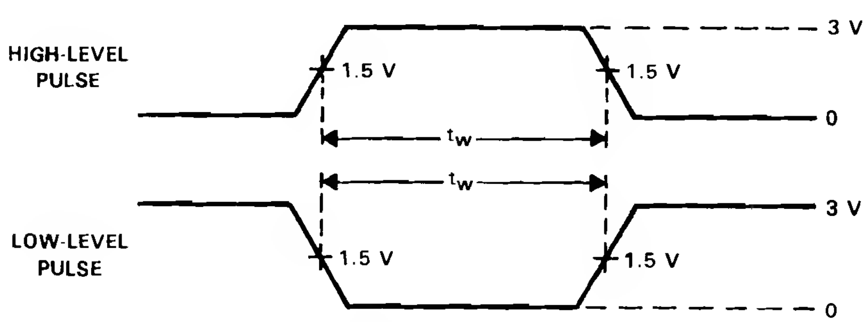
VOLTAGE WAVEFORMS

FIGURE 3. SETUP AND HOLD TIMES, AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS

FIGURE 4. ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS



VOLTAGE WAVEFORMS

FIGURE 5. PULSE DURATIONS

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = t_f = 2 ns.
B. For clock inputs, f_{max} is measured with input duty cycle = 50%
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

special design features

True CMOS Outputs: Each TICPAL22V10Z output is designed with a P-channel pull-up transistor and an N-channel pull-down transistor, a true CMOS output with rail-to-rail output switching. This provides direct interface to CMOS logic, memory, or ASIC devices without the need for a pull-up resistor. The CMOS output has 16-mA drive capability, which makes the TICPAL22V10Z an ideal substitute for bipolar PLDs. The electrical characteristics of this device show the output under both CMOS and TTL conditions.

Simultaneous Switching: High-performance CMOS devices often have output glitches on nonswitched outputs when a large number of outputs are switched simultaneously. This glitch is commonly referred to as "ground bounce" and is most noticeable on outputs held at V_{OL} (low-level output voltage). Ground bounce is caused by the voltage drop across the inductance in the package lead when current is switched ($dv \propto I \times di/dt$).

One solution is to restrict the number of outputs that can switch simultaneously. Another solution is to change the device pinout such that the ground is located on a low-inductance package pin. TI opted for a third option in order to maintain pinout compatibility and eliminate functional constraints. This option controls the output transistor turn-on characteristics and puts a limit on the instantaneous current available to the load, much like the I_{OS} resistor in a TTL circuit.

Wake-Up Features: The TICPAL22V10Z employs input signal transition detection techniques to power-up the device from the standby-power mode. The transition detector monitors all inputs, I/Os, and feedback paths. Whenever a transition is sensed, the detector activates the power-up mode. The device will remain in the power-up mode until the detector senses that the inputs and outputs have been static for about 40 ns; thereafter, the device returns to the standby mode.

Turbo Mode or Zero-Power Mode: When the turbo cell is programmed, the device will be set to the power-up mode. Therefore, the delay associated with its transition detection and power up will be eliminated. This is how the faster propagation delays and shorter setup times are obtained in the turbo mode. The turbo mode and the associated speed increase can be effectively simulated with the turbo cell erased, if a series of adjacent input, I/O, or feedback edges occur with an interval of about 25 ns or less between these adjacent edges. Under these conditions, the TICPAL22V10Z will never have the opportunity to power down due to the frequency of the adjacent edges.

Power Dissipation: Power dissipation of the TICPAL22V10Z is defined by three contributing factors, and the total power dissipation is the sum of all three.

Standby Power: The product of V_{CC} and the standby I_{CC}. The standby current is the reverse current through the diodes that are reversed biased. This current is very small, and for circuits that remain in static condition for a long time, this low amount of current can become a major performance advantage.
Dynamic Power: The product of V_{CC} and the dynamic current. This dynamic current flows through the device only when the transistors are switching from one logic level to the other. The total dynamic current for the TICPAL22V10Z is dependent upon the users' configuration of the PAL and the operating frequency. Output loading can be a source of additional power dissipation.
Interface Power: The product of I_{CC} (interface) and V_{CC}. The total interface power is dependent on the number of inputs at the TTL V_{OH} level. The interface power can be eliminated by the addition of a pull-up resistor.

Even though power dissipation is a function of the user's device configuration and the operating frequency, the TICPAL22V10Z is a lower powered solution than either the quarter-powered or half-powered bipolar devices. The virtually zero standby power feature makes the TICPAL22V10Z the device of choice for low-duty-cycle and battery-powered applications.

programming and erasability

Programming of the TICPAL22V10Z is achieved through floating-gate avalanche injection techniques. The charge trapped on the floating gate remains after power has been removed, allowing for the nonvolatility of the programmed data. The charge can be removed by exposure to light with wavelengths of less than 400 nm (4000 Å). The recommended erasure wavelength is 253.7 nm (2537 Å), with erasure time of 60 to 90 minutes, using a light source with a power rating of 12000 $\mu W/cm^2$ placed within 2.5 cm (1 inch) of the device.

The TICPAL22V10 is designed for programming endurance of 1000 write/erase cycles with a data retention of ten years. To guarantee maximum data retention, the window on the device should be covered by an opaque label. The fluorescent light in a room can erase a unit in three years or, in the case of a direct sunlight, erasure can be complete in one week.

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

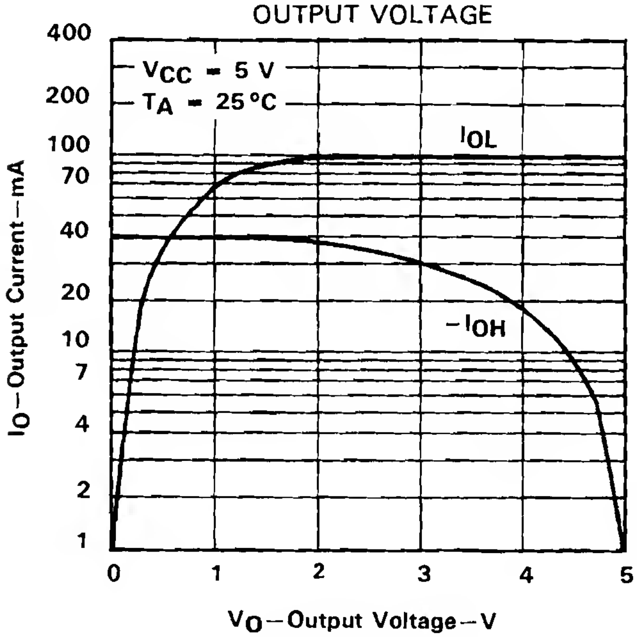


FIGURE 6

NORMALIZED SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE
(10-BIT COUNTER)

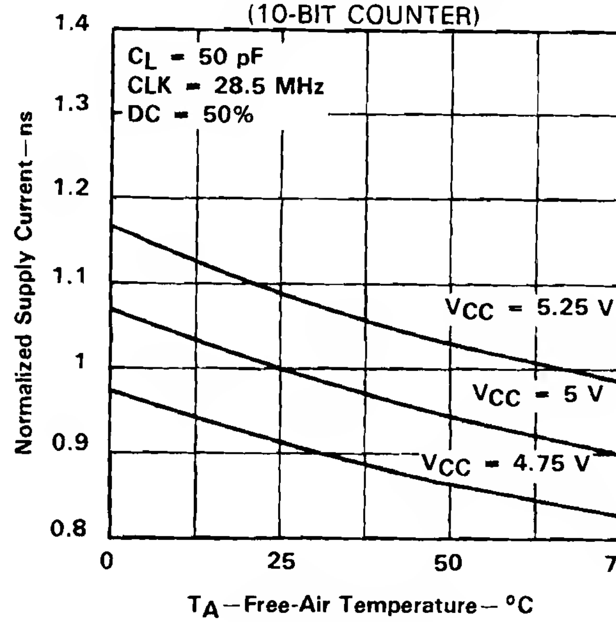


FIGURE 7

SUPPLY CURRENT
vs
CLOCK FREQUENCY
(10-BIT COUNTER)

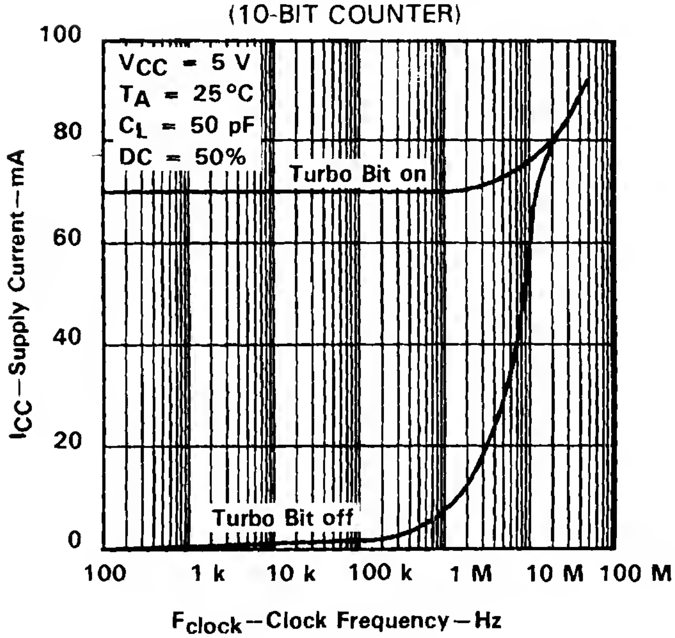


FIGURE 8

NORMALIZED PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

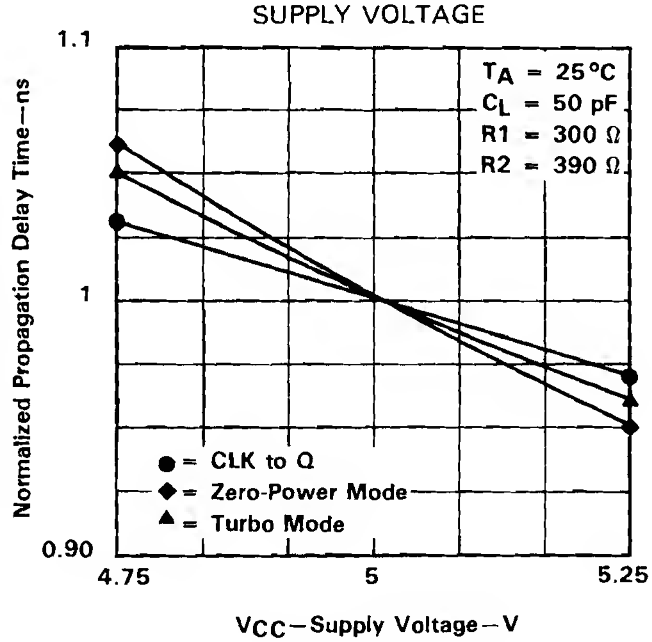


FIGURE 9

NORMALIZED PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

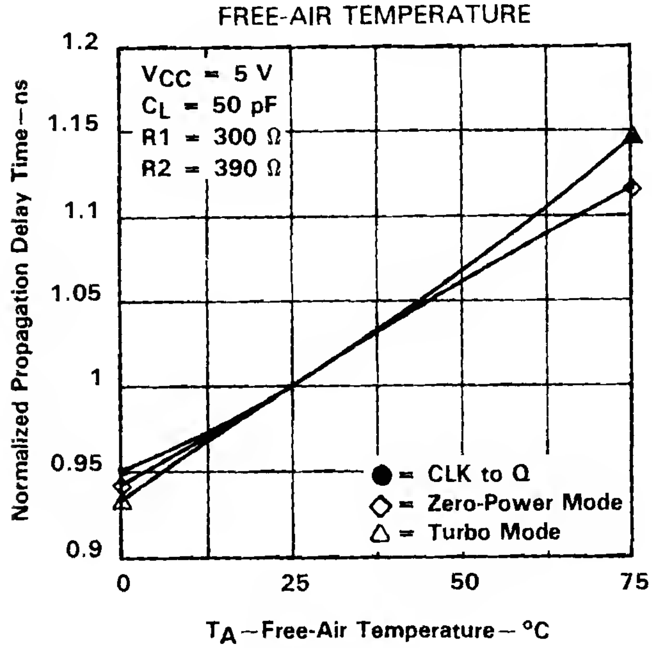


FIGURE 10

DELTA PROPAGATION TIME
vs
LOAD CAPACITANCE

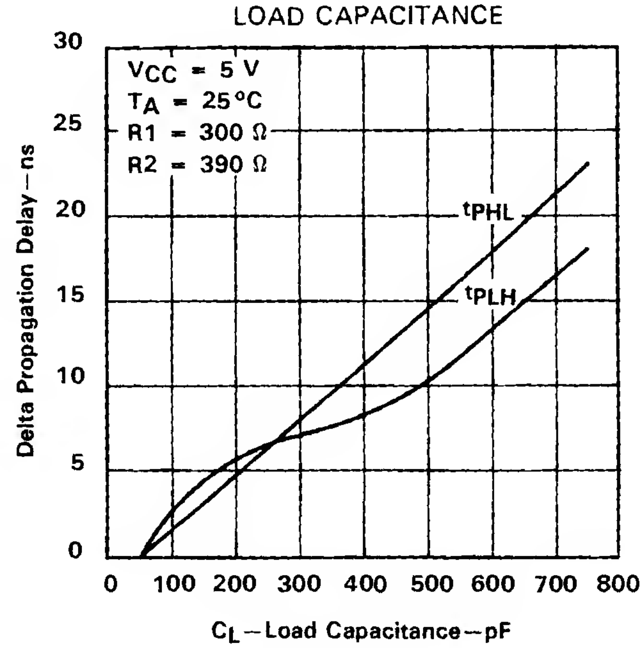


FIGURE 11

DELTA PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

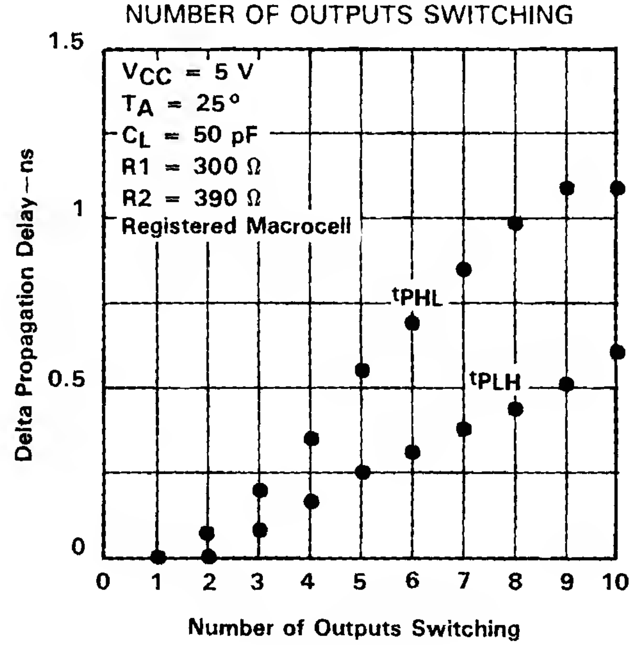


FIGURE 12

3349131 10997566 PAL HC7

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